Response to request for Information on Function Details of:
Multiple Logical Channel Subsystem

- MCSS (introduced in the z990 2084 family) and the Multi Image Facility (MIF).

I did not detail the functions of I wanted to target the TidBit on terms and definitions. Here is the background as I understand it, although I am 'not' an SME on this topic.

In order to achieve the necessary increase in the total I/O capacity of the z system, several z/Architecture constraints had to be addressed and redefined in a manner that minimizes their impact on providing more than 256 channels and associated I/O devices to the z operating systems, such as z/OS, z/VM, z/Linux, the zSeries Transaction Processing Facility (TPF), and the VSE/ESA operating systems, that execute in the logical partitions configured to a z system. Specifically, the architecturally defined channel-path identification number, called the channel-path identifier (CHPID), had to be maintained without change. The CHPID value is defined as an 8-bit binary number resulting in a range of unique CHPID values from 0 to 255; therefore, a maximum of 256 channel paths were possible on previous S/370, S/390, and z/Architecture-class systems.

Since the inception of the precursor S/370 XA channel-subsystem architecture in the late 1970s, this 8-bit CHPID has been maintained without change because of its pervasive use in the z/OS and z/VM operating systems. For example, the CHPID value is maintained in many internal programming control blocks, is displayed in various operator messages, and is the object of various system commands, programming interfaces, etc., all of which would have to be redesigned if the CHPID value was increased to more than an 8-bit number in order to accommodate more than 256 channel paths.

In addition to increasing the total number of channel paths that may be configured to a z-class system, configuring a corresponding increase in the number of I/O devices to a large mainframe system was necessary.

In z/Architecture, each I/O device is represented by a separate set of controls, called subchannels, which are used by the channel subsystem to activate, monitor, and report the progress of I/O operations for their associated I/O device. Prior to MCSS, the z/Architecture provided a maximum of 64K subchannels and an equal maximum number of I/O devices. As was true with the limited number of channel paths on previous S/390 and zSeries systems, this 64K maximum I/O device limitation had to be removed in a manner that caused minimal disruption to the zSeries operating systems and their associated application programs. Therefore, the MCSS facility, xtended the z/Architecture CSS to provide up to 65,280 channel paths.

Here how it works -
1. An additional level of channel-path-addressing indirection is created that allows more than 256 physical channel paths to be installed and uniquely identified without changing the legacy 8-bit CHPID value and the corresponding programming dependencies on the CHPID. This new channel-path-identification value, called the physical-channel identifier (PCHID), is a 16-bit binary number ranging from 0 to 65,279, which uniquely identifies each physically installed channel path. With the z990 and above, a current maximum of 1024 external channel paths (e.g., ESCON*, FICON*, OSA) and 48 internal channel paths (e.g., Internal Coupling and IQDIO hyperlink) are each assigned a unique PCHID value in the range of 0 to 2,047. With

the exception of the I/O configuration program (IOCP) and the dynamic I/O configuration programming, both of which are used to create and modify the z channel subsystem I/O configurations, the PCHID value is transparent to the programs operating in each LPAR. Correspondingly, both of these I/O configuration management programs are enhanced to provide the controls necessary to associate the PCHID value of each channel path with its corresponding CHPID values.

2. The physical CSS is restructured into multiple "logical" channel subsystems. Each logical CSS is called a channel subsystem image, and each image is identified by a unique 8-bit binary number ranging from 0 to 254, called the channel-subsystem-image identifier (CSSID), resulting in an architecture maximum of 256 channel subsystem images per central processor complex (CPC) footprint. Additionally, each CSS image may be configured with a maximum of 256 unique channel paths, called a channel-path set (CPS). This results in an architecture maximum of 64K physical channel paths for a given CPC footprint.

Each channel-subsystem image is also structured to provide its own z/Architecture MIF. The multipleimage facility (previously supported by some S/390 and all previous z/Architecture models) that is associated with each channel subsystem image provides for the replication of both channel-path and subchannel controls. This is necessary to allow each of the logical partitions that are configured to a given channelsubsystem image to have its own set of I/O controls in order to dynamically access and share up to 256 physical channel paths and up to 64K physical I/O devices that may be attached to the channel paths configured to the channel-subsystem image.

3. The multiple-image facility is also extended in order to allow physical channel paths to be defined and concurrently configured to multiple channel-subsystem images. Such shared channel paths are called "spanned" channel paths because they allow the channel paths and their attached I/O devices to be dynamically and transparently shared by programs operating in LPARs which are configured to different channel-subsystem images; that is, they span multiple channel-subsystem images.