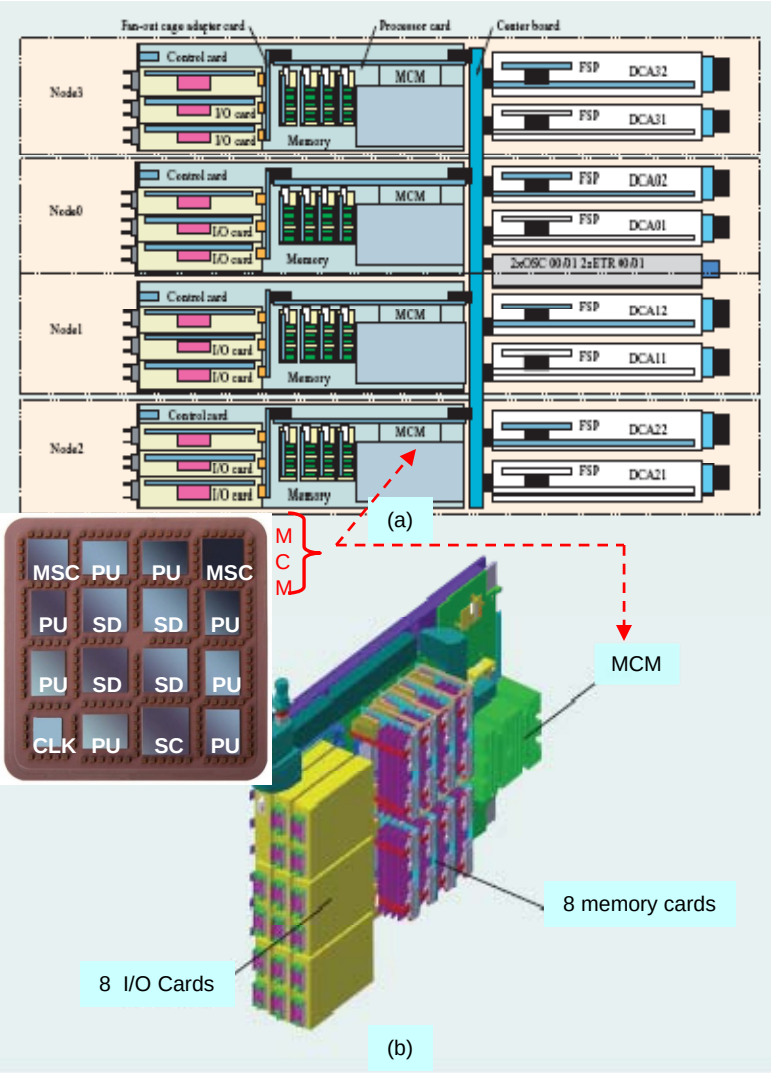
Official

z9 Cheat Sheet

(Logical System Structure)



(a) CEC packaging (top view); (b) processor node packaging.

zCPO – JK
Ref: z9 SJ

- The node-based server design of the System z9 accommodates up to **32** processor chips, or **64** processor cores, per system.
- The system memory size can be increased up to a maximum of 512 GB, and the system I/O connectivity has been enhanced to a maximum of 64 self-timed interface (STI) I/O paths, each with a capability of 2.27 Gb/s.
- The increase in number of processors, memory size, and connectivity allows us to achieve the desired symmetrical multiprocessor (SMP) performance, but it generates a significant increase in the total number of interconnections between chips.
- The 64-processor system is divided into four processor cards (nodes).
- Each processor card contains 16 dual-core processors on an MCM, up to 128 GB of main memory and 16 STI interfaces.
- The processor chip is connected to each cache chip by a 16-byte bus operated at 1.72 Gb/s.
  - This results in a bandwidth of 441 GB/s on a single node.
- Up to four nodes are plugged into the center board using connectors each with 1,160 signal pins.
  - The connector holds the ring of the processor nodes and feeds the power into the processr cards.
  - The high-speed interconnections of the EI connect the cache chips on the MCM with the cache chips on the other processor cards to ensure fast access of all cache data to each CPU.
  - The bus speed is 0.86 Gb/s for a single line, with a total bandwidth of 124 GB/s.
  - A jumper card closes the ring in a two- or three-node configuration.
- The MCM also provides the connection to the memory via the memory storage controllers (MSCs).
  - A maximum of eight memory cards can be plugged per node; each memory card contains four dual inline memory modules (DIMMs) and two storage memory interface (SMI) control chips.
  - The interfaces are operated at a fixed gear ratio of 2:1 with respect to the processor cycle time.
- The eight I/O slots per node are provided by the fanout cage adapter card.
  - They connect a high-speed GXþ bus (running at half the processor frequency) from each slot to the two MSC chips on the MCM.
- The I/O card holds the memory bus adapter (MBA) module, which converts the GX+bus into two 2.27-GB/s fast unidirectional STI links.
  - The STI I/O connection is used to connect to z9* I/O cages or other zSeries systems.
  - The two STI cable channels per card result in 16 STI links per processor card and up to 64 STI I/O paths per system.
- The processor node is controlled by a system control card in the fan-out cage.
  - This card provides the control structure for the processor and I/O cards.
  - It controls the configuration and power-on sequence, as well as the error handling of the node.
  - There are redundant communication paths via the serial interface from the flexible service processor (FSP) cards in the distributed converter assemblies (DCAs).
- Two high-availability redundant DCAs provide redundant power supplies for each processor card.
  - One FSP card, hosted in the DCA, controls one processor card, and the second FSP, hosted in the second DCA, is for redundancy.
  - A maximum of eight DCA cards with eight FSP daughter cards are used in each central electronic complex (CEC) cage.
- Two redundant oscillator (OSC) cards are plugged into the z9 center board.
  - One card is always active, while the other is a redundant backup.
  - The dynamic oscillator switch modules on the two OSC cards communicate with each other, switching the clock generation to the other card at a failure of the master for redundancy.
  - Each card provides a clock signal generator for various master clocks at the clock chip in CEC.
  - All four processor cards are controlled by the same OSC card.
- Two redundant external time reference (ETR) cards are implemented to allow the z9 to be coupled to another z9 system.
  - One card is always active, while the other one is a redundant backup.
  - Each card provides the ETR optical receiver function for the clock chip on the processor MCM.